AMENDMENTS TO THE CLAIMS

1. (Currently amended) A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer is configured to generate equalized data; and

a clock and data recovery circuit coupled to the decision feedback equalizer, wherein the clock and data recovery circuit is configured to generate an extracted clock signal from the equalized data,

wherein the decision feedback equalizer includes:

a retimer that is configured to generate recovered equalized data from the equalized data in response to the extracted clock signal; and

a multiplier coupled to the retimer, the multiplier being configured to apply an equalization coefficient to the recovered equalized data to generate [[the]] an equalized feedback signal;

wherein the clock and data recovery circuit is configured to iterate the equalization coefficient until the clock and data recovery circuit synchronizes with a frequency of the equalized data.

2. (Currently amended) The communications system of claim 1 wherein the decision feedback equalizer comprises a summer that is configured to generate a combined signal by combining [[an]] the equalized feedback signal with the received data.

3. (Previously presented) The communications system of claim 2 wherein:

the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer is configured to generate the equalized data by converting the combined signal into a binary signal; and

the clock and data recovery circuit is configured to generate the extracted clock signal from the binary signal.

4. (Currently amended) The communications system of claim 3 wherein:

the retimer comprises a ~~flip-flop~~ flip-flop coupled to the slicer and to the clock and data recovery circuit; and

the ~~flip-flop~~ flip-flop is configured to generate the recovered equalized data from the binary signal in response to the extracted clock signal.

5. (Previously presented) The communications system of claim 3 wherein:

the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop,

the frequency acquisition loop is configured to adjust a frequency of the extracted clock signal to maintain a fixed relationship between a frequency of a reference signal and the frequency of the extracted clock signal, and

the phase lock loop is configured to adjust a phase of the extracted clock signal to maintain a fixed relationship between a phase of the binary signal and the phase of the extracted clock signal.

6. (Previously presented) The communications system of claim 5 wherein the clock and data recovery circuit further comprises a frequency lock detector configured to determine when the frequency of the extracted clock signal is fixed relative to the frequency of the reference signal.

7-16. (Canceled)

17. (Previously presented) A communications system comprising:

a decision feedback equalizer comprising:

a summer that is configured to combine an equalized feedback signal with the received data,

a slicer coupled to the summer, the slicer being configured to convert the combined signal to a binary signal,

a retimer coupled to the slicer, the retimer being configured to generate recovered equalized data from the binary signal in response to an extracted clock signal, and

a multiplier coupled to the retimer, the multiplier being configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and

a clock and data recovery circuit coupled to the slicer, the clock and data recovery circuit being configured to:

generate the extracted clock signal from the binary signal; and

vary the equalization coefficient based on a difference between a divided frequency of the extracted clock signal and a frequency of a reference clock.

18. (Currently amended) The communications system of claim 17 wherein:

the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop, the frequency acquisition loop being configured to adjust the frequency of the extracted clock signal to maintain a fixed relationship between [[a]] the frequency of the reference clock and the frequency of the extracted clock signal, and

the phase lock loop is configured to adjust a phase of the extracted clock signal to maintain a fixed relationship between a phase of the binary signal and the phase of the extracted clock signal.

19. (Previously presented) The communications system of claim 18 wherein the clock and data recovery circuit further comprises a frequency lock detector configured to determine when the frequency of the extracted clock signal is fixed relative to the frequency of the reference clock.

20-26. (Canceled)

27. (Previously presented) The communications system of claim 1, wherein the equalization coefficient is based on a bit error rate of the received data.

28. (Previously presented) The communications system of claim 1, wherein

the clock and data recovery circuit is configured to adjust the equalization coefficient based on a frequency difference exceeding a threshold, the frequency difference being based on a frequency of a reference clock included in the clock and data recovery circuit and a frequency of a divided signal, the divided signal being generated from the extracted clock signal.

29-32. (Canceled)